Ultralow Noise Microphone with Bottom Port and PDM Digital Output

Data Sheet

ADMP521

FEATURES

Small and thin 4 mm × 3 mm × 1 mm surface-mount package
Omnidirectional response
Very high SNR: 65 dBA
Sensitivity of −26 dBFS
Extended frequency response from 100 Hz to 16 kHz
Low current consumption: 900 µA
Sleep mode for extended battery life, <1 µA consumption
120 dB maximum SPL
High PSR of −80 dBFS
Fourth-order Σ-Δ modulator
Digital PDM output
Compatible with Sn/Pb and Pb-free solder processes
RoHS/WEEE compliant

APPLICATIONS

Smartphones and feature phones
Tablet computers
Teleconferencing systems
Digital still and video cameras
Bluetooth headsets
Notebook PCs
Security and surveillance

FUNCTIONAL BLOCK DIAGRAM

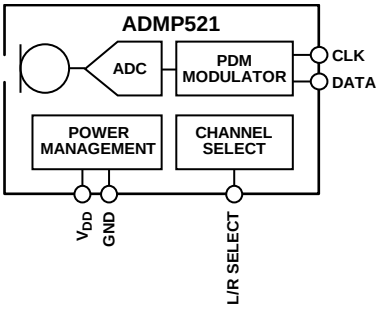

Figure 1.

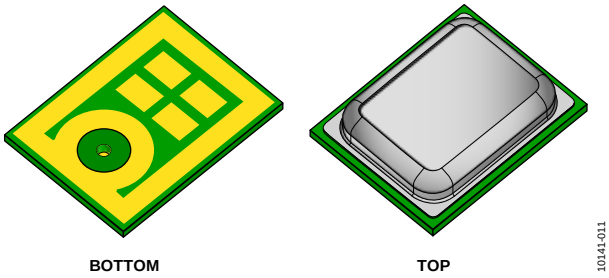

Figure 2. Isometric Views of ADMP521 Microphone Package

GENERAL DESCRIPTION

The ADMP521[1] is a high performance, ultralow noise, low power, digital output, bottom-ported omnidirectional MEMS microphone. The ADMP521 consists of a MEMS microphone element and an impedance converter amplifier followed by a fourth-order sigma-delta (Σ-Δ) modulator. The digital interface allows for the pulse density modulated (PDM) output of two microphones to be time-multiplexed on a single data line using a single clock. The ADMP521 is function and pin compatible with the ADMP421 microphone, providing an easy upgrade path.

The ADMP521 has a very high signal-to-noise ratio (SNR) and common sensitivity of −26 dBFS, making it an excellent choice for far field applications. The ADMP521 has an extended wideband frequency response resulting in natural sound with high intelligibility. Low current consumption and a sleep mode with less than 1 µA current consumption enables long battery life for portable applications. The ADMP521 complies with the TIA-920 *Tele-communications Telephone Terminal Equipment Transmission Requirements for Wideband Digital Wireline Telephones* standard.

The ADMP521 is available in a thin 4 mm × 3 mm × 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation. The ADMP521 is halide free.

[1] Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; 7,961,897. Other patents are pending.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

4/12—Rev. 0 to Rev. A

Changes to General Description Section ... 1
Changed Supply Voltage Min Parameter from 1.65 V to 1.8 V ... 3
Changed 500 Hours to 1000 Hours in Table 7 ... 14

2/12—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{DD} = 1.8 V, CLK = 2.4 MHz, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PERFORMANCE					
Directionality			Omni		
Sensitivity[1]	1 kHz, 94 dB sound pressure level (SPL)	−29	−26	−23	dBFS
Signal-to-Noise Ratio (SNR)	20 Hz to 20 kHz, A-weighted		65		dBA
Equivalent Input Noise (EIN)	20 Hz to 20 kHz, A-weighted		29		dBA SPL
Dynamic Range	Derived from EIN and maximum acoustic input		91		dB
Frequency Response[2]	Low frequency −3 dB point		100		Hz
	High frequency −3 dB point		16		kHz
	Deviation limits from flat response within pass band		−3/+8		dB
Total Harmonic Distortion (THD)	105 dB SPL			2.5	%
Power Supply Rejection (PSR)	217 Hz, 100 mV p-p sine wave superimposed on V_{DD} = 1.8 V		−80		dBFS
Maximum Acoustic Input	Peak		120		dB SPL
POWER SUPPLY					
Supply Voltage (V_{DD})		1.8		3.3	V
Supply Current (I_S)					
Normal Mode	V_{DD} = 1.8 V		0.9	1.0	mA
	V_{DD} = 3.3 V		1.0	1.2	mA
Sleep Mode[3]	V_{DD} = 1.8 V			0.5	µA
	V_{DD} = 3.3 V			0.8	µA
DIGITAL INPUT/OUTPUT CHARACTERISTICS					
Input Voltage High (V_{IH})		0.65 × V_{DD}			V
Input Voltage Low (V_{IL})				0.35 × V_{DD}	V
Output Voltage High (V_{OH})	I_{LOAD} = 0.5 mA	0.7 × V_{DD}	V_{DD}		V
Output Voltage Low (V_{OL})	I_{LOAD} = 0.5 mA		0	0.3 × V_{DD}	V
Output DC Offset	Percent of full scale		7		%
Latency			<30		µs
Noise Floor	20 Hz to 20 kHz, A-weighted		−91		dBFS

[1] Relative to the rms level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.
[2] See Figure 7 and Figure 8.
[3] The microphone enters sleep mode when clock frequency is less than 1 kHz.

TIMING CHARACTERISTICS

Table 2.

Parameter	Description	Min	Typ	Max	Unit
SLEEP MODE					
Sleep Time	Time from CLK falling < 1 kHz		1		ms
Wake-Up Time	Time from CLK rising > 1 kHz, power on		10		ms
INPUT					
t_{CLKIN}	Input clock period	326		800	ns
Clock Frequency (CLK)		1.25	2.4[1]	3.072	MHz
Clock Duty Ratio		40		60	%
OUTPUT					
t_{1OUTEN}	DATA1 (right) driven after falling clock edge	40			ns
$t_{1OUTDIS}$	DATA1 (right) disabled after rising clock edge	5		30	ns
t_{2OUTEN}	DATA2 (left) driven after rising clock edge	40			ns
$t_{2OUTDIS}$	DATA2 (left) disabled after falling clock edge	5		30	ns

[1] The microphone operates at any clock frequency between 1.0 MHz and 3.3 MHz. Some specifications may not be guaranteed at frequencies other than 2.4 MHz.

Timing Diagram

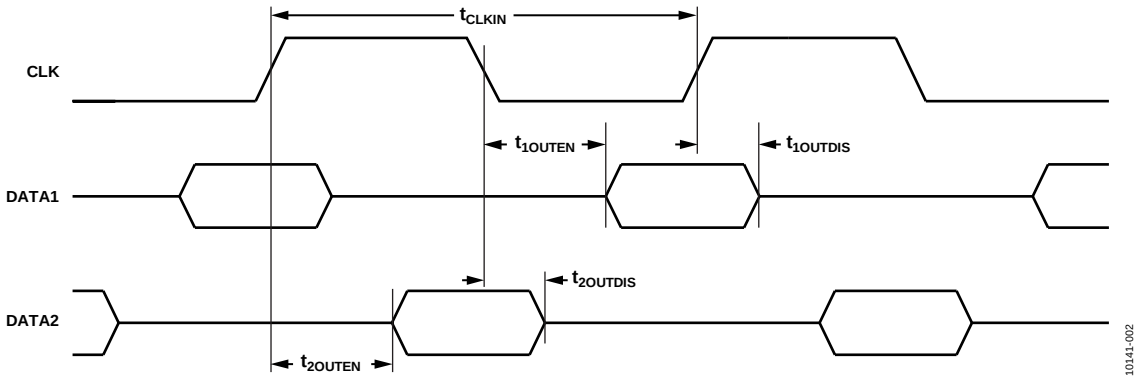

Figure 3. Pulse Density Modulated Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
Digital Pin Input Voltage	−0.3 V to V_{DD} + 0.3 V or +3.6 V, whichever is less
Sound Pressure Level	160 dB
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	−40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

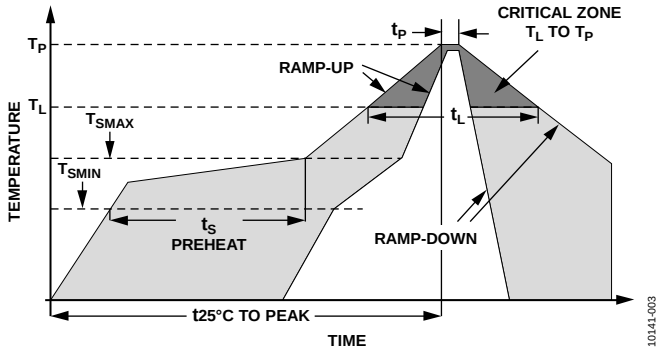

Figure 4. Recommended Soldering Profile Limits

Table 4. Recommended Soldering Profile Limits

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	1.25°C/sec maximum	1.25°C/sec maximum
Preheat		
Minimum Temperature (T_{SMIN})	100°C	100°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)	1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)	45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)	183°C	217°C
Peak Temperature (T_P)	215°C +3°C/−3°C	260°C + 0°C/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate	3°C/sec maximum	3°C/sec maximum
Time 25°C (t25°C) to Peak Temperature	5 minute maximum	5 minute maximum

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

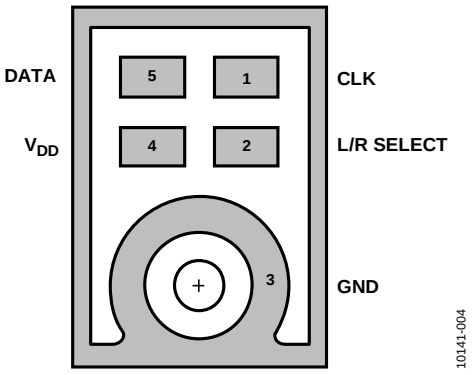

Figure 5. Pin Configuration (Bottom View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input to Microphone.
2	L/R SELECT	Left Channel or Right Channel Select. DATA1 (right): L/R SELECT tied to GND. DATA2 (left): L/R SELECT pulled to V_{DD}.
3	GND	Ground.
4	V_{DD}	Power Supply. Placing a 0.1 µF (100 nF) ceramic type X7R capacitor between Pin 4 (V_{DD}) and ground is strongly recommended for best performance and to avoid potential parasitic artifacts. Place the capacitor as close to Pin 4 as possible.
5	DATA	Digital Output Signal (DATA1, DATA2).

TYPICAL PERFORMANCE CHARACTERISTICS

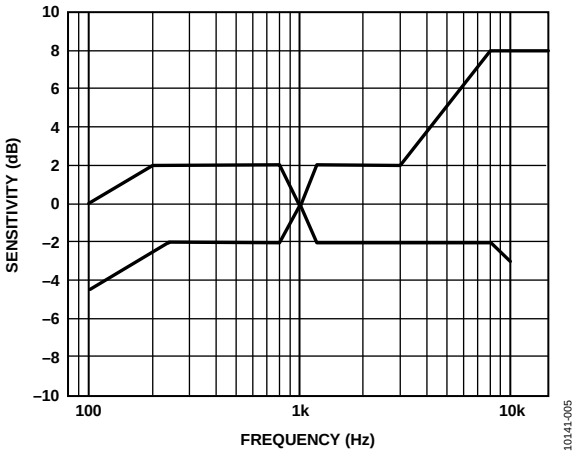

Figure 6. Frequency Response Mask

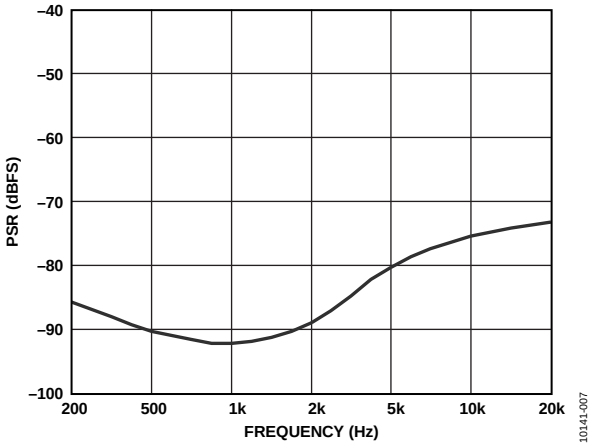

Figure 8. Typical PSR vs. Frequency

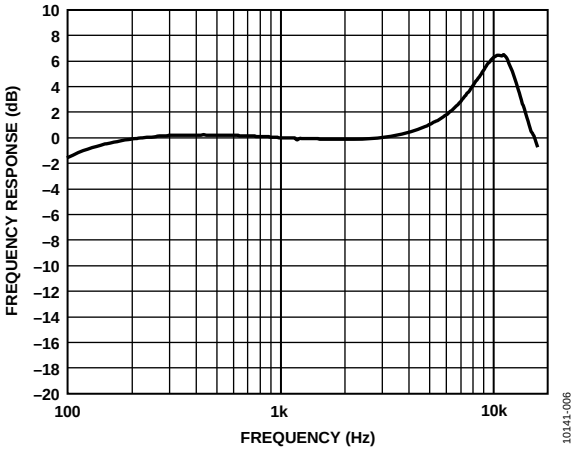

Figure 7. Typical Frequency Response (Measured)

THEORY OF OPERATION

PDM DATA FORMAT

The output from the DATA pin of the ADMP521 is in PDM format. This data is the 1-bit output of a fourth-order Σ-Δ modulator. The data is encoded so that the left channel is clocked on the falling edge of CLK and the right channel is clocked on the rising edge of CLK. After driving the DATA signal high or low in the appropriate half frame of the CLK signal, the DATA driver of the microphone tristates. In this way, two microphones, one set to the left channel and the other to right, can drive a single DATA line. See Figure 3 for a timing diagram of the PDM data format; the DATA1 and DATA2 lines shown in this figure are two halves of the single physical DATA signal. Figure 10 shows a diagram of the two stereo channels sharing a common DATA line.

If only one microphone is connected to the DATA signal, the output is only clocked on a single edge (see Figure 9). For example, a left channel microphone is never clocked on the rising edge of CLK. In a single microphone application, each bit of the DATA signal is typically held for the full CLK period until the next transition because the leakage of the DATA line is not enough to discharge the line while the driver is tristated.

See Table 6 for the channel assignments according to the logic level on the L/R SELECT pin.

Table 6. ADMP521 Channel Setting

L/R SELECT Setting	Channel
Low (tie to ground)	DATA1 (right)
High (tie to V_{DD})	DATA2 (left)

For PDM data, the density of the pulses indicates the signal amplitude. A high density of high pulses indicates a signal near positive full scale and a high density of low pulses indicates a signal near negative full scale. A perfect zero (dc) audio signal shows an alternating pattern of high and low pulses.

The output PDM data signal has a small dc offset of between 3% to 7% of full scale. This dc signal is typically removed by a high-pass filter in the codec that is connected to the digital microphone.

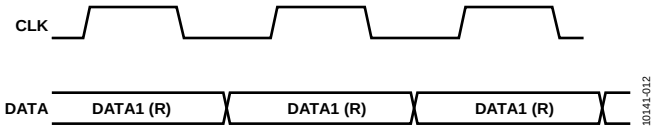

Figure 9. Mono PDM Format

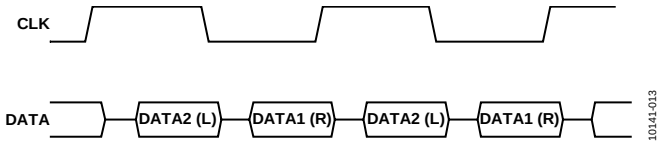

Figure 10. Stereo PDM Format

PDM MICROPHONE SENSITIVITY

The acoustic input levels of the microphone in dB SPL are rms measurements; however, the sensitivity and output level of a digital microphone is given as a peak level. This is because its output is referenced to the full-scale digital word, which is a peak value. This convention is different from the output levels of analog microphones, which are given as an rms voltage. The ADMP521 has a sensitivity of −26 dBFS. A 94 dB SPL (rms) input signal gives a −26 dBFS peak output level; therefore, the rms level of this digital output is −29 dBFS.

This convention of using peak levels to specify the output of digital microphones must be kept in mind when configuring downstream signal processing that may rely on precise signal levels. For example, dynamic range processors (compressors, limiters, noise gates) typically set thresholds based on rms signal levels; therefore, adjust the signals of the microphone from peak to rms by lowering the dBFS value by 3 dB.

CONNECTING PDM MICROPHONES

A PDM output microphone is typically connected to a codec with a dedicated PDM input. This codec separately decodes the left and right channels and filters the high sample rate modulated data back to the audio frequency band. This codec also generates the clock for the PDM microphones or is synchronous with the source that is generating the clock. See the Applications Information section for additional details on connecting the ADMP521 to Analog Devices, Inc., audio codecs with a PDM input. Figure 11 and Figure 12 show mono and stereo connections of the ADMP521 and a codec. The mono connection shows an ADMP521 set to output data on the right channel. To output on the left channel, tie the L/R SELECT pin to V_{DD} instead of GND.

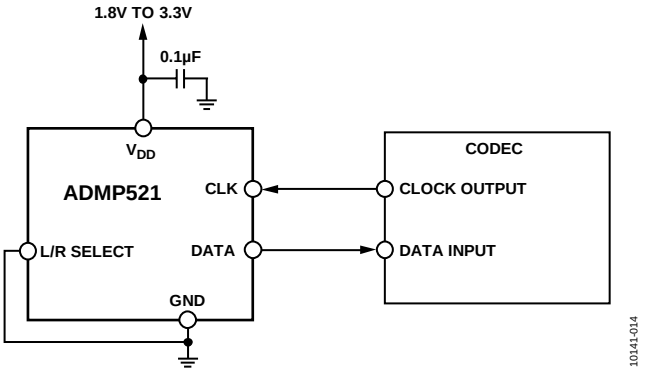

Figure 11. Mono PDM Microphone (Right Channel) Connection to Codec

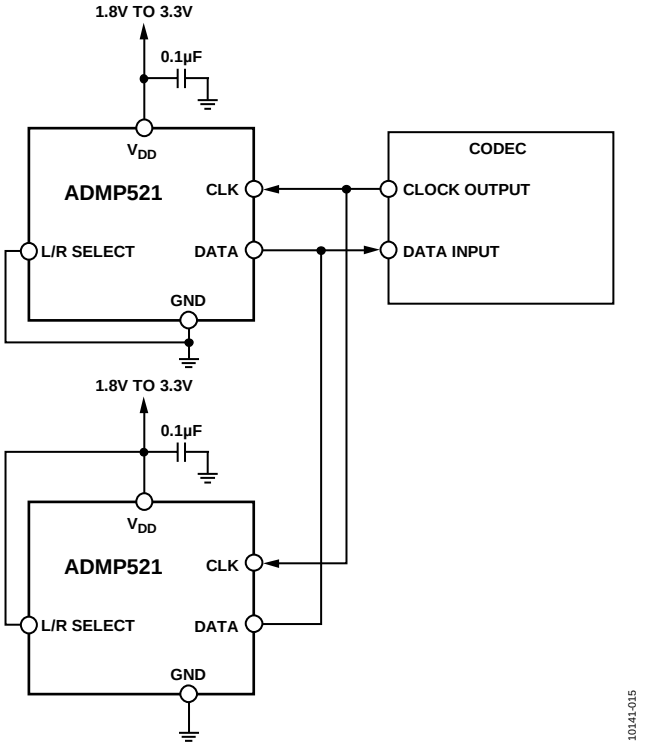

Figure 12. Stereo PDM Microphone Connection to Codec

Decouple the V_{DD} pin of the ADMP521 to GND with a 0.1 µF capacitor. Place this capacitor as close to V_{DD} as the printed circuit board (PCB) layout allows.

Do not use a pull-up or pull-down resistor on the PDM data signal line because it can pull the signal to an incorrect state during the period that the signal line is tristated.

The DATA signal does not need to be buffered in normal use when the ADMP521 microphone(s) is placed close to the codec on the PCB. If the ADMP521 needs to drive the DATA signal over a long cable (>15 cm) or other large capacitive load, a digital buffer may be needed. Only use a signal buffer on the DATA line when one microphone is in use or after the point where two microphones have been connected (see Figure 13). The DATA output of each microphone in a stereo configuration cannot be individually buffered because the two buffer outputs cannot drive a single signal line. If a buffer is used, take care to select one with low propagation delay so that the timing of the data connected to the codec is not corrupted.

When long wires are used to connect the codec to the ADMP521, a 100 Ω source termination resistor may be used on the clock output of the codec instead of a buffer to minimize signal overshoot or ringing. Depending on the drive capability of the codec clock output, a buffer may still be needed, as shown in Figure 13.

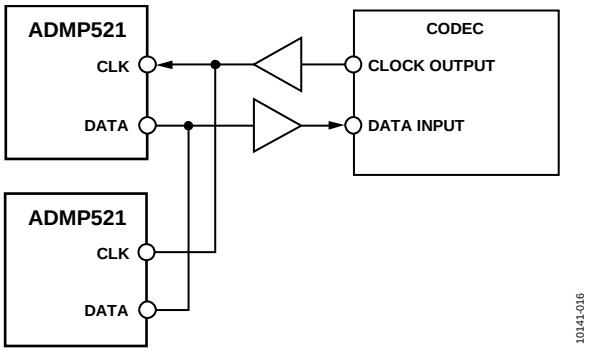

Figure 13. Buffered Connection Between Stereo ADMP521s and a Codec

SLEEP MODE

The microphone enters sleep mode when the clock frequency falls below 1 kHz. In this mode, the microphone data output is in a high impedance state. The current consumption in sleep mode is less than 1 µA.

The ADMP521 enters sleep mode within 1 ms of the clock frequency falling below 1 kHz. The microphone wakes up from sleep mode in 32,768 cycles after the clock becomes active. With a 3.072 MHz clock, the microphone wake time is 10.7 ms; for a 2.4 MHz clock, the microphone wake time is 13.7 ms.

START-UP

The start-up time of the ADMP521 from when the clock is active is the same time as the waking from sleep time. The microphone starts up 32,768 cycles after the clock is active.

APPLICATIONS INFORMATION

INTERFACING WITH ANALOG DEVICES CODECS

The PDM output of the ADMP521 interfaces directly with the digital microphone inputs on Analog Devices ADAU1361, ADAU1761, and ADAU1781 codecs. See the connection diagram shown in Figure 14, and refer to the AN-1003 Application Note and the respective data sheets of the codecs for more details on the digital microphone interface.

The CN-0078 Circuit Note describes the connection between these codecs and a digital microphone. All configuration information is the same for the ADMP521 as it is for the ADMP421.

SUPPORTING DOCUMENTS

For additional information, see the following.

Evaluation Board User Guides

UG-326, *EVAL-ADMP521Z-FLEX: Bottom-Ported, Digital Output, MEMS Microphone Evaluation Board*

UG-335, *EVAL-ADMP521Z Bottom Port Digital Output MEMS Microphone Evaluation Board*

Circuit Note

CN-0078, *Digital MEMS Microphone Simple Interface to a SigmaDSP Audio Codec*

Application Notes

AN-1003, *Recommendations for Mounting and Connecting Analog Devices, Inc., Bottom-Ported MEMS Microphones*

AN-1068, *Reflow Soldering of the MEMS Microphone*

AN-1112, *Microphone Specifications Explained*

AN-1124, *Recommendations for Sealing Analog Devices, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress*

AN-1140, *Microphone Array Beamforming*

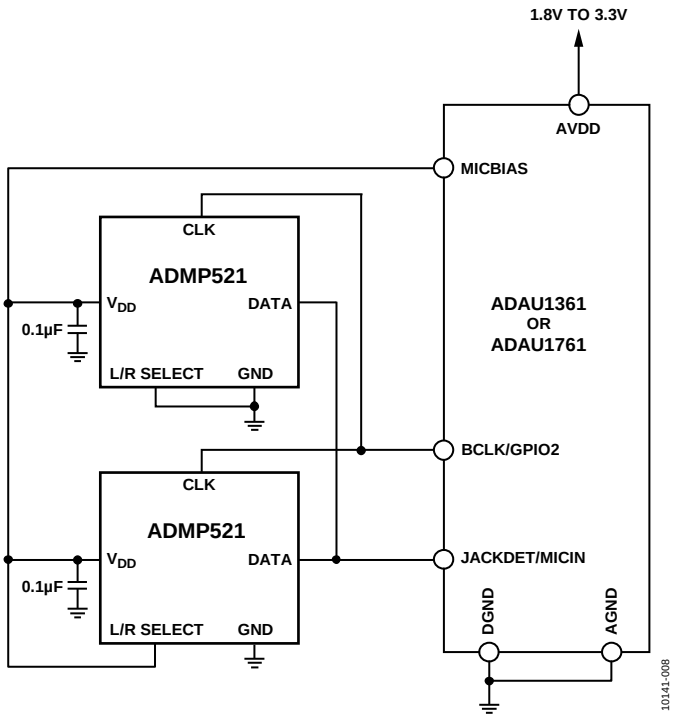

Figure 14. ADAU1361 or ADAU1761 Stereo Interface Block Diagram

PCB DESIGN AND LAYOUT

The recommended PCB land pattern for the ADMP521 should be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 15. Take care to avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 16.

The response of the ADMP521 is not affected by the PCB hole size as long as the hole is not smaller than the sound port of the microphone (0.25 mm, or 0.010", in diameter). A 0.5 mm to 1 mm (0.020 inch to 0.040 inch) diameter for the hole is recommended. Take care to align the hole in the microphone package with the hole in the PCB. The exact degree of the alignment does not affect the microphone performance as long as the holes are not partially or completely blocked.

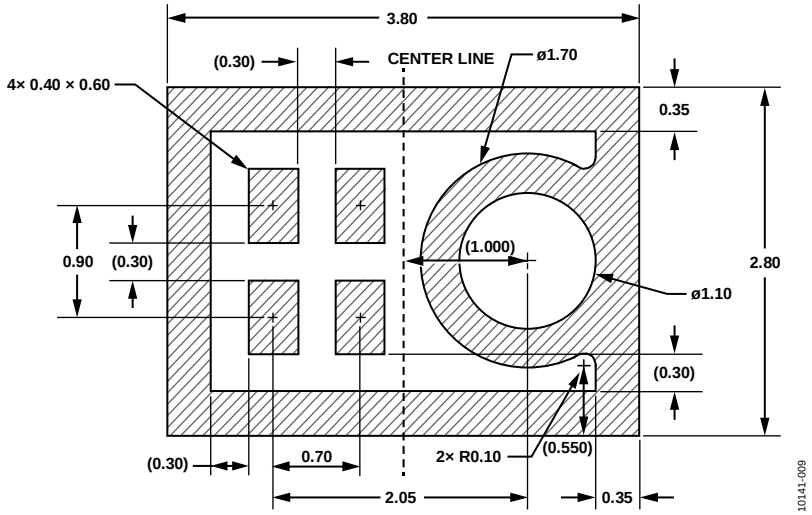

Figure 15. Suggested PCB Land Pattern Layout

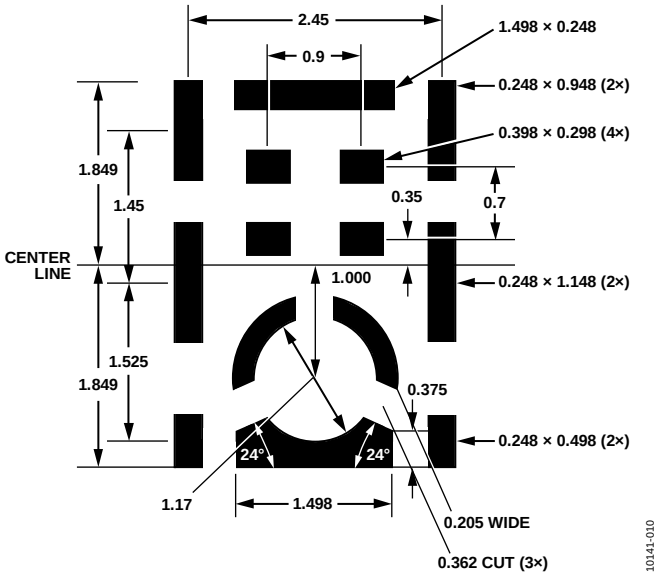

Figure 16. Suggested Solder Paste Stencil Pattern Layout

ALTERNATIVE PCB LAND PATTERNS

The standard PCB land pattern of the ADMP521 has a solid ring around the edge of the footprint that may make routing the microphone signals more difficult in some board designs. This ring is used to improve the RF immunity performance of the ADMP521; however, it is not necessary to have this full ring connected for electrical functionality. If a design can tolerate reduced RF immunity, this ring can either be broken or removed completely from the PCB footprint. Figure 17 shows an example PCB land pattern with no enclosing ring around the edge of the part, and Figure 18 shows an example PCB land pattern with the ring broken on two sides so that the inner pads can be more easily routed on the PCB.

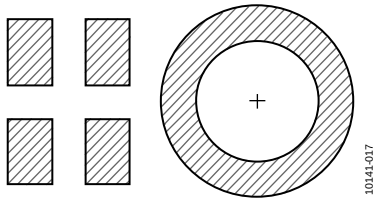

Figure 17. Example PCB Land Pattern with No Enclosing Ring

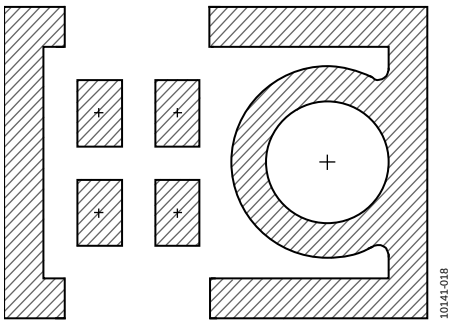

Figure 18. Example PCB Land Pattern with Broken Enclosing Ring

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground. If a pattern like one of these two examples is used on a PCB, take care that the unconnected ring on the bottom of the ADMP521 is not placed directly over any exposed copper. This ring on the microphone is still at ground and any PCB traces routed underneath it need to be properly masked to avoid short circuits.

PCB MATERIAL AND THICKNESS

The performance of the ADMP521 is not affected by PCB thickness and can be mounted on both a rigid and flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port, while providing the shortest acoustic path for good sound quality.

HANDLING INSTRUCTIONS

PICK-AND-PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Use care during pick-and-place to ensure that no high shock events above 10 kg are experienced because such events may cause damage to the microphone.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile should be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 4 and Table 4.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures and ultrasonic cleaning.

RELIABILITY SPECIFICATIONS

The microphone sensitivity after stress must deviate by no more than 3 dB from the initial value.

Table 7.

Stress Test	Description
Low Temperature Operating Life	−40°C, 1000 hours, powered
High Temperature Operating Life	+125°C, 1000 hours, powered
Temperature Humidity Bias (THB)	+85°C/85% relative humidity (RH), 1000 hours, powered
Temperature Cycle	−40°C/+125°C, one cycle per hour, 1000 cycles
High Temperature Storage	150°C, 1000 hours
Low Temperature Storage	−40°C, 1000 hours

OUTLINE DIMENSIONS

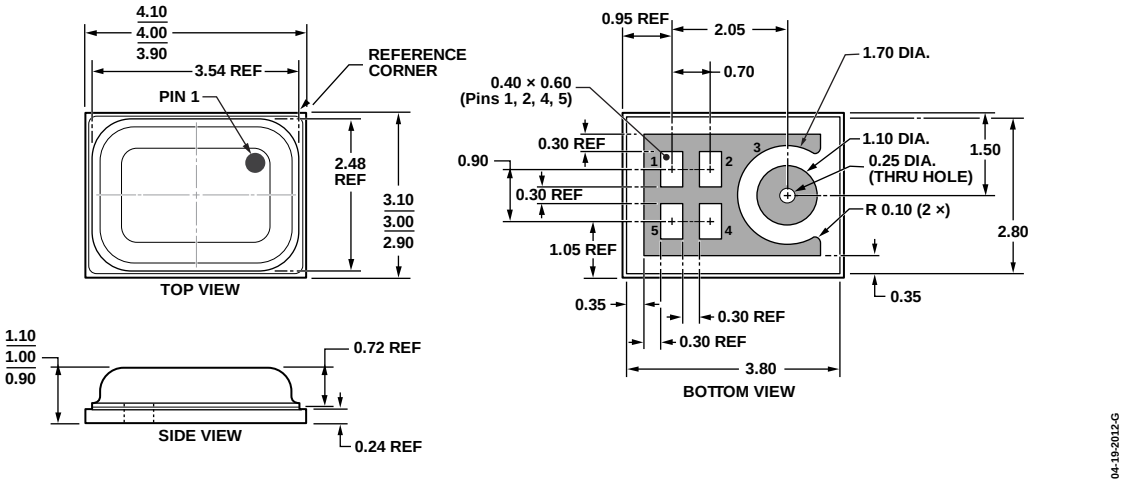

Figure 19. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4 mm × 3 mm Body
(CE-5-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]	Ordering Quantity
ADMP521ACEZ-RL	−40°C to +85°C	5-Terminal LGA_CAV, 13″ Tape and Reel	CE-5-1	5,000
ADMP521ACEZ-RL7	−40°C to +85°C	5-Terminal LGA_CAV, 7″ Tape and Reel	CE-5-1	1,000
EVAL-ADMP521Z		Evaluation Board		
EVAL-ADMP521Z-FLEX		Flexible Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] This package option is halide free.

NOTES

D10141-0-4/12(A)